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EXAMINER	
NGUYEN, TANH Q	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 06/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/603,797	HONMURA, TETSUROO	
	Examiner	Art Unit	
	Tanh Q. Nguyen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 16 is objected to because of the following informalities:

"comprised" on line 2 of claim 16 should be replaced with "comprises".

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

3. Claims 9-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 9 recites the limitation "wherein the address selection circuit sends an error signal to the address selection circuit" in lines 9-10 is confusing, as it is not clear how the address selection circuit can send an error signal to itself.

Claim 10 recites the limitation "a fourth start address in a fourth memory address belonging to the first memory space" in lines 3-4 is confusing, as it is not clear whether there is a difference between the fourth start address and the fourth memory address.

Claim 10 recites the limitation "the first protocol decode and generation circuit receives the first memory range" in lines 10-11 is confusing, as it is not clear whether the first memory range and the third memory range are the same.

The rejections that follow are based on the examiner's best interpretation of the claims.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 15-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Takeda (US 6,292,851).

6. As per claim 15, Takeda teaches a semiconductor integrated circuit [2, FIG. 1] comprising:

a first CPU [12, FIG. 1] accessing a first memory space with address translations [PHYSICAL ADDRESS SPACE, FIG. 10] and a second memory space without address translations [MEMORY ADDRESS SPACE, FIG. 10];

a peripheral LSI [6 - FIG. 1], separate from the first CPU, to transfer data between said first CPU and a peripheral device [17, FIG. 1], said peripheral LSI comprising;

an address translation circuit [22, 32 -` FIG. 2];

a nonvolatile memory [30, FIG. 2] to store address information indicating a relationship between an address of the first memory space and an address of the second memory space [col. 5, lines 22-24];

a first protocol decode and generation circuit [22, 24, 34 - FIG. 2] connecting to a first bus [IN, OUT, 36, 38, 40 - FIG. 2] connected to the first memory space; and

a second protocol decode and generation circuit [22, 20 - FIG. 2] connecting to a second bus [8, FIG. 2] connected to the second memory space;

wherein the address translation circuit is connected to the first and second protocol decode and generation circuits and comprises:

a register [32, FIG. 2], and

an address calculation circuit [22, FIG. 2].

7. As per claim 16, Takeda teaches the peripheral LSI further comprising a flexible bus controller [16, FIG. 2] which includes said address translation circuit and said first and second protocol decode and generation circuits.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 5-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeda.

10. As per claim 5, Takeda further teaches when the semiconductor integrated circuit acts as a bus master to access the first memory space (when CPU 12 acts as a master to access the PHYSICAL ADDRESS SPACE), the second protocol decode and generation circuit receives a first address in the second memory space (when

supervisory interface circuit 20 receives an address in the MEMORY ADDRESS SPACE) and sends the first address to the address calculation circuit, the address calculation circuit translates the first address into a second address in the first memory space using an address conversion table stored in the non-volatile memory [col. 5, lines 22-24], and the address calculation circuit sends the second address to the first protocol decode and generation circuit [converted address is used by parallel I/O 34 to access the peripheral device].

Takeda therefore disclosed the claimed invention except for the address calculation unit translating the first address stored in the register into the second address in the first memory space from address information stored in a register of the translation unit, the address information being read from the nonvolatile memory when the semiconductor integrated circuit is initialized.

Essentially, Takeda teaches translation using a look-up table for address translation, whereas the claimed invention uses a formula for address translation, wherein the second address = first address + the first start address - the second start address.

Since it was known in the art at the time the invention was made to perform address translation from a first address space to a second address space using either a look-up table, or a formula with the start address of a first address space, and the start address of a second address space (the start addresses being parameters known at initialization), it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform address translation using a formula with known

parameters, as an alternative to performing address translation using a look-up table - hence using a register to store the first start address and the second start address at initialization and performing address translation using the start addresses stored in the register.

11. As per claim 6, Takeda teaches the address information being changed in the nonvolatile memory (hence stored in the nonvolatile memory) when the physical addresses of the functional modules are changed, e.g. when engineering changes are made to the semiconductor integrated circuit [col. 6, line 67-col. 7, line 2; col. 6, lines 60-62], and the nonvolatile memory being modifiable by on-board reprogramming [col. 7, lines 32-34].

Since a probing test is normally conducted in association with an engineering change, and since the nonvolatile memory is modifiable by on-board reprogramming, it would have been obvious to one of ordinary skill in the art at the time the invention was made to store the address information in the nonvolatile memory (by on-board reprogramming) when a probing test (associated with an engineering change) is conducted is on the semiconductor integrated circuit in order to reflect a proper relationship between the address of the first memory space and the address of the second memory space, and in order to allow Takeda's system to function properly.

12. As per claims 7-8, see the rejections of claim 5 above.

13. As per claim 9, since it was known in the art at the time the invention was made to define the range of a memory space to ensure proper address translation, and to send an error signal when an address is out-of-range, it would have been obvious to

one of ordinary skill in the art at the time the invention was made for the nonvolatile memory to store the address width for defining the first memory range, and for the address translation circuit to comprise a selection circuit and an interrupt circuit in order to send an error signal to the selection circuit when an address is out of range.

14. As per claim 10, Takeda teaches a plurality of peripheral devices [17, FIG. 1], hence teaches a third start address in a third memory range of the MEMORY ADDRESS SPACE and a fourth start address in a fourth memory range of the PHYSICAL ADDRESS SPACE.

15. As per claims 12-14, see the rejections of claim 16 above.

Response to Arguments

16. Applicant's arguments with respect to claims 5-16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

17. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tanh Q. Nguyen whose telephone number is 571-272-4154. The examiner can normally be reached on M-F 9:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

June 12, 2006

TQN
June 12, 2006